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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/696,560

10/30/2003

Eric R. Fossum

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03/13/2006

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP

2101 L Street, NW

Washington, DC 20037

EXAMINER

PYO, KEVIN K

ART UNIT

PAPER NUMBER

2878

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/696,560

Applicant(s)

FOSSUM, ERIC R.

Examiner

Kevin Pyo

Art Unit

2878

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-53 is/are pending in the application.
- 4a) Of the above claim(s) 10-16, 26-32 and 42-48 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 17-25, 33-41 and 49-53 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>5/20/04</u> .   | 6) <input type="checkbox"/> Other: _____                                    |

***Election/Restrictions***

1. Applicant's election with traverse of Group I (Fig.2; claims 1-9, 17-25, 33-41 and 49-53) in the reply filed on 12/29/2005 is acknowledged.

In response to applicant's argument that claim 53 is generic to the inventions of Group I and II, the Examiner disagrees with this argument. Claim 53 is not generic claim to Group II because claim 10 does not recite all the limitations of claim 53. The claims of the first species (claims 1-9, 17-25, 33-41 and 49-53) and claim 53 are examined together since claim 53 reads on the elected species.

In response to applicant's argument that, in view of MPEP 803, no serious burden will be imposed on the examiner because the inventions associated with Figs.2 and 4 are closely related to each other, it was not found persuasive because the Election of Species requirement issued on 11/30/2005 is based on the fact that the claimed invention has patentably distinct species, not the criteria under MPEP 803. Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence not of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either case, if the examiner finds one of the invention unpatentable over the prior art, the evidence of admission can be used in a rejection under 35 USC 103(a) of the other invention.

The requirement is still deemed to be proper and is therefore mad FINAL.

The elected claims (claims 10-16, 26-32 and 42-48) should be canceled in view of expediting the prosecution.

***Claim Rejections - 35 USC § 112***

2. Claims 1-9, 17-25 and 33-41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 1, 17 and 33, these claims recite “a first storage **node** for **storing** a reset voltage” and “a second storage **node** for **storing** a voltage” (emphasis added). It is unclear how the recited voltage could be stored into “a node”. Is it well known in the art? Clarification is required.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-9, 17-25, 33-41 and 49-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Yadid-Pecht et al (6,515,702).

Regarding claims 1, 17, 33 and 53, as far as the claim is understood, Yadid-Pecht et al shows in Figs.1-3 the following elements of applicant's invention: a plurality of pixels (Fig.2), wherein each of said pixels (col.2, lines 36-52) comprises a reset portion (45, RST) for resetting a photosensitive element of said pixel, a first storage node (a reset sample and hold circuit in the

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readout circuit 70; Fig.3) for storing a reset voltage level of said photosensitive element and a second storage node (a signal sample and hold circuit in the readout circuit 70; Fig.3) for storing a voltage level of said photosensitive element after an integration period. Regarding claim 33, it would be inherent that the imaging device of Yadid-Pecht et al comprises a processor.

Regarding claims 2, 18 and 34 the limitation therein is disclosed in col.6, lines 9-13.

Regarding claims 3, 19 and 35, as far as the claim is understood, Yadid-Pecht et al shows in Fig.3 a reset sample and hold circuit and a signal sample and hold circuit are coupled to a column bus.

Regarding claims 4, 5, 20, 21, 36 and 37 Yadid-Pecht et al shows in Fig.3 a first sample and hold circuit (a reset sample and hold circuit) comprising the recited first sample and hold transistor (225) and the recited storage capacitor (230).

Regarding claims 6, 22 and 38, Yadid-Pecht et al shows in Fig.3 a first terminal of a first storage capacitor (230) is coupled to a gate of a first source follower transistor (240), a first source/drain terminal of the first source follower transistor is coupled to a supply voltage terminal (Vss) and a second source/drain terminal of the first source follower transistor is switchably coupled to the column bus with a column select transistor (245).

Regarding claims 7, 8, 23, 24 39 and 40, Yadid-Pecht et al shows in Fig.3 a second sample and hold circuit (a signal sample and hold circuit) comprising the recited first sample and hold transistor (200) and the recited storage capacitor (205).

Regarding claims 9, 25 and 41, Yadid-Pecht et al shows in Fig.3 a first terminal of a second storage capacitor (205) is coupled to a gate of a second source follower transistor (210), a first source/drain terminal of the second source follower transistor is coupled to a supply voltage

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terminal (Vss) and a second source/drain terminal of the second source follower transistor is switchably coupled to the column bus with a column select transistor (220).

Regarding claims 49-52, the method steps recited therein are inherently disclosed by the device of Yadid-Pecht et al.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Pyo whose telephone number is (571) 272-2445. The examiner can normally be reached on Mon-Fri (with flexible hour), First Mon. off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Y. Epps can be reached on (571) 272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Kevin Pyo  
Primary Examiner  
Art Unit 2878

Pkk  
3/7/06